II. REMARKS

Claims 1-8, 10-23, 25, 27, 30-32, and 36-38 are pending. In the February 02, 2005 response, the Applicants' attorney amended claims 1, 12, 21-23, 25, 27, 30, 32, and 36-37, cancelled claims 9, 24, 26, 28-29, and 33-35 without prejudice or disclaimer, and added new claim 38. In light of the following, all of the claims as amended are now in condition for allowance, and, therefore, the Applicants' attorney requests the Examiner to withdraw all of the outstanding rejections. But if after considering this response the Examiner does not allow all the claims, the Applicant's attorney requests that the Examiner contact him to schedule a teleconference to further the prosecution of the application.

Rejection of Claims 1-15 and 21 Under 35 U.S.C. § 102(b) As Being Anticipated By U.S. Patent 5,852,583 to Taito et al.

In the February 02, 2005 response, the Applicants' attorney indicated that remarks in support of the patentability for claims 1-15 and 21 would follow in this Supplemental Amendment. Below are these remarks.

Claim 1 as amended is directed to a line selector for a matrix of memory elements.

The line selector comprises a plurality of matrix line group selection circuits, each one allowing the selection of a respective group of matrix lines according to a first address, each matrix line group including at least one plurality of matrix lines.

Associated with each matrix line group selection circuit, a respective plurality of matrix line selection circuits is provided. Each matrix line selection circuit allows the selection of at least one respective matrix line within the respective matrix line group, according to a second address; the matrix line selection circuits comprise matrix line driver circuits for driving potentials of the matrix lines.

Flag means are associated with each matrix line group: the flag means that are associated with the generic matrix line group can be set to declare a pending status of a prescribed operation to be conducted globally on the memory elements of the

respective matrix line group. The flag means enable, when set, the execution of the prescribed operation on the memory elements of the respective matrix line group.

Furthermore, means are provided for entrusting the flag means with the selection of the respective matrix line group during the execution of the prescribed operation, in alternative to the respective line group selection circuit.

For example, as described in the patent application, the claimed matrix line selector allows implementing in a selective way an operation that normally has a global character, such as an erase of the memory elements (memory cells) in the matrix. In particular, the selectivity is by groups of matrix lines (e.g., word lines). The selectivity is achieved in a rather simple way, and with minor changes to conventional matrix line selectors; for example, word line selectors having at least a first-level decoder and a second-level decoder are quite usual in the field of memory ICs. The matrix line selector also allows implementing a simple sectorization scheme of the memory: each matrix line group can in fact be considered as a memory sector, *e.g.* erasable individually and independently from the other memory sectors: in this way, the number of unnecessary erase pulses applied to the memory cells is on the average reduced, with a benefit on the memory aging.

Taito et al. (US 5,852,583) describe (Fig. 1) a semiconductor memory device comprising, for each word line (WL00-WL03, WL10-WL13), a respective *word line drive unit* (WD00-WD03, WD10-WD13).

The generic *word line drive unit* includes an *AND circuit* (01) *receiving an address to generate a predecode signal* (RAU0).

A *predecode signal* (RAL0) *output from a predecode signal generation unit* (PSC0) (buffered by an inverter B0) and a signal (denoted IPGM) which is asserted (low) in program, are fed to a *select signal output unit* (two transfer gates formed by MOSFETs labelled TN01 and TP01, and TN02 and TP02, respectively).

The *select signal output unit* is responsive to the *predecode signal* RAU0 and provides, as a *select signal* (WLS0) either the *predecode signal output* RAL0, or the signal IPGM. A *word line driver* (D0) is *responsive to select signal* WLS0 *to activate word line* WL00.

Further provided are a *latch circuit* (L0) for latching the select signal WLS0 to activate the respective word line, and a *transfer gate* (TG0) *for disconnecting latch circuit L0 and word line driver D0 from the select signal output unit.*

Claim 1 as amended distinguishes over the structure disclosed by *Taito et al.* The differences appear once a correct parallel is established between the elements of the claim and the circuits of *Taito et al.*

In particular, the claimed plurality of matrix line group selection circuits may find correspondence in the *predecode signal generation units* PSC0 and PSC1: considering the generic one of these units, *e.g.* PSC0, the *predecode signal* RAL0 is common to all the word lines of the group WL00-WL03.

Similarly, the claimed plurality of matrix line selection circuits is provided, associated with each matrix line group selection circuit, each matrix line selection circuit allowing the selection of at least one respective matrix line within the respective matrix line group, according to a second address, and comprising matrix line driver circuits for driving potentials of the matrix lines, find correspondence in the *word line drive units* WD00-WD03, and WD10-WD13.

It can thus be appreciated that in *Taito et al.* there is nothing corresponding to the claimed flag means that are associated with each matrix line group, that can be set to declare a pending status of a prescribed operation to be conducted globally on the memory elements of the respective matrix line group, and that enable, when set, the execution of the prescribed operation on the memory elements of the respective matrix line group. In *Taito et al.* each of the *word line drive units* WD00-WD03, and WD10-WD13, that is, each one of the circuit blocks which are associated with and control selection of one respective word line WL00-WL03, and WL10-WL13, includes respective *latches*, like L0, L1. Only one of these latches is set in a read, program or erase operation to be carried out on the respective, single word line. Differently from the claimed circuit, in *Taito et al.* there are instead no flag means that are associated with each matrix line group and that, when set, enable the execution of the prescribed operation globally on the memory elements of the respective matrix line group.

As a matter of fact, *Taito et al.* seem not concerned with operations that are to be conducted globally on the memory elements of the respective matrix line group: only

operations carried out on a selected single word line at a time are considered. The problem faced by *Taito et al.* seems to have been one of reducing the parasitic capacitance for the predecode signals like RAL0 and RAL1.

Similar reasoning applies to amended method claim 11. As mentioned above, *Taito et al.* seem not concerned with operations that are to be conducted globally on the memory elements of a matrix line group, and only operations carried out on a selected single word line at a time are considered.

Conclusion

In light of the foregoing, claims 2-8, 10-11, 13-20, and 31 as previously pending, claims 1, 12, 21-23, 25, 27, 30, 32, and 36-37 as amended and new claim 38 added in our February 02, 2005 response, are in condition for full allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicant's attorney, Bryan Santarelli, at (425) 455-5575.

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Respectfully Submitted,

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